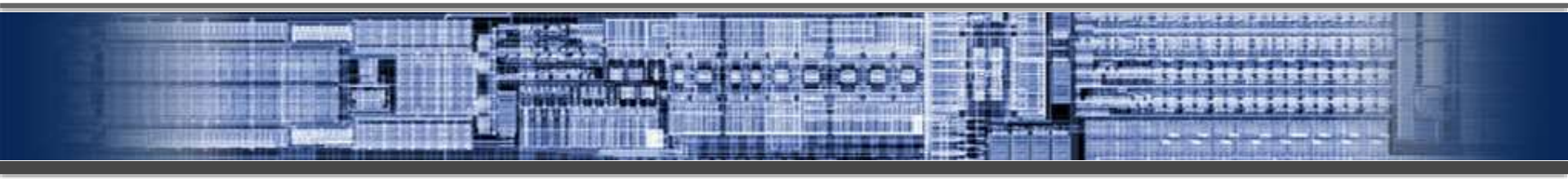


Pushing the limits of performance for clocking systems using microwatts of system power from 5nm to 180nm

Andrew Cole, VP at Silicon Creations

Outline

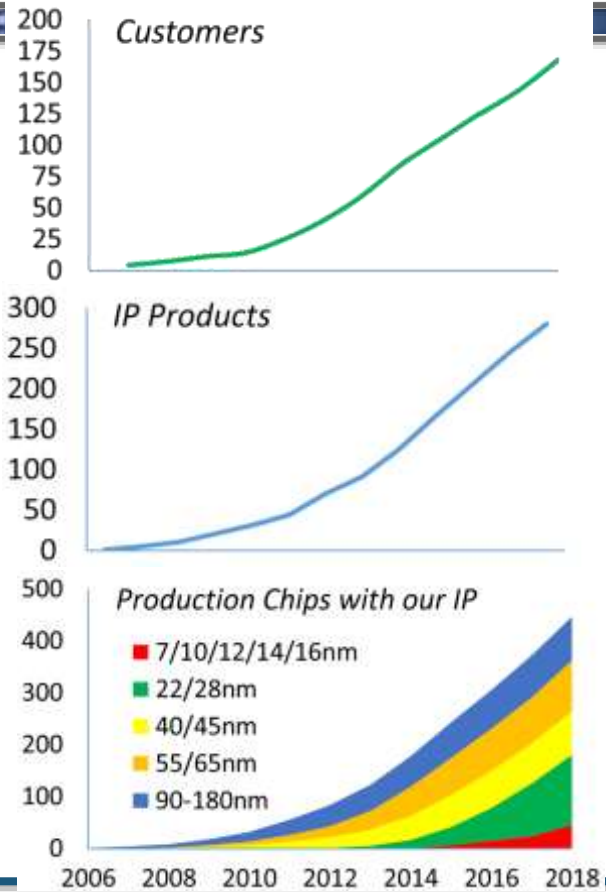
- Silicon Creations introduction
- PLL optimizations … extreme low energy for IoT
- Challenges of doing this in 5nm
- Correlating Simulation and Silicon Results
- Summary

Silicon Creations Overview

- IP provider of PLLs, Oscillators and High-speed Interface
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- >165 customers (>65 in China)
- Mass production from 7nm to >180nm, 5nm coming soon

Company Statistics

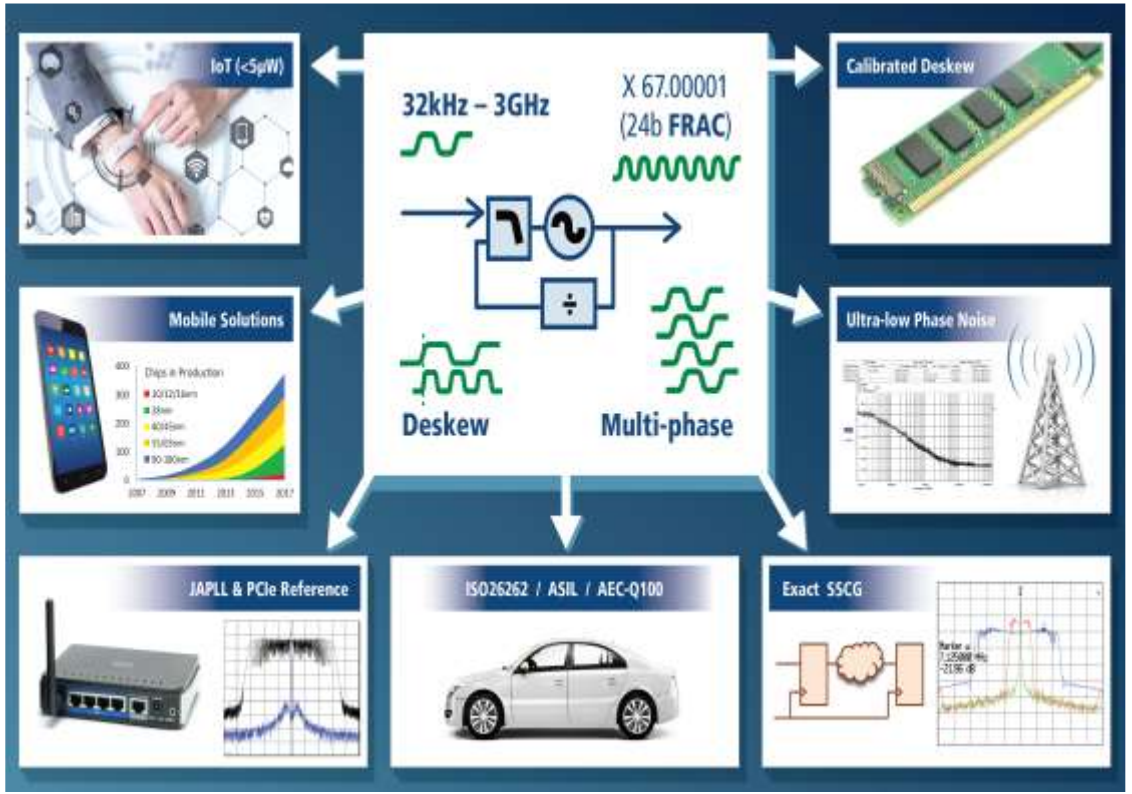
- Since 2006, Silicon Creations has provided over 300 analog/mixed-signal IP designs, from TSMC 350nm down to 5nm
  - ~170 customers
  - 170 different PLL designs
  - 9 PLL/Oscillator IPs in TSMC 7FF
  - 400+ customer chips with our IP in production at TSMC
- Silicon Creations target all segments
  - Consumer, Mobile, TV/displays, Set-top boxes, Data Center, IoT, Automotive, Aerospace, Industrial, …



PLLs from Silicon Creations

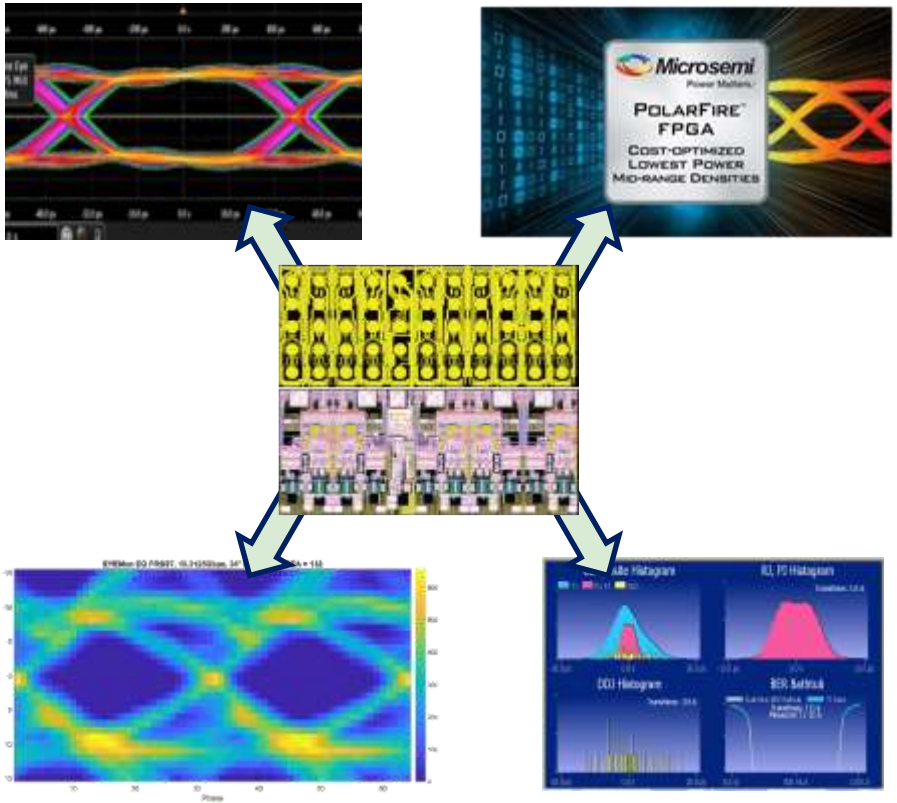
- Highest volume analog IPs – robust design and good QA are essential
  e.g.
  - TSMC 28nm FRAC PLL >116 MP tapeouts, >833k wafers, >2B PLLs
  - TSMC 16FFC FRAC PLL >43 MP tapeouts, >828k wafers, >2B PLLs

- PLL products include general purpose, fractional, low jitter AFE, µW IoT, Automotive



SerDes from Silicon Creations

- Robust and proven from 28nm to 180nm and from <100Mbps to >20Gbps
- Multiprotocol (for FPGA) and targeted protocols
  - SGMII, XAUI, RapidIO, V-by-1 HS/US, FastLVDS, CameraLink, FPDLink, OIF-CEI, JESD204, CPRI, PCIe1-3, 10G-KR, …



Lab Testing

Test lab with Matlab controlled equipment – 12 benches

> 100 IP test reports from 7nm to 180nm

Awards for quality & support

- 2017
  - Audience choice paper, USA OIP
  - Mixed-Signal IP Partner of the year
- 2014
  - Best Emerging IP vendor
- 2012
  - Audience choice paper, USA OIP

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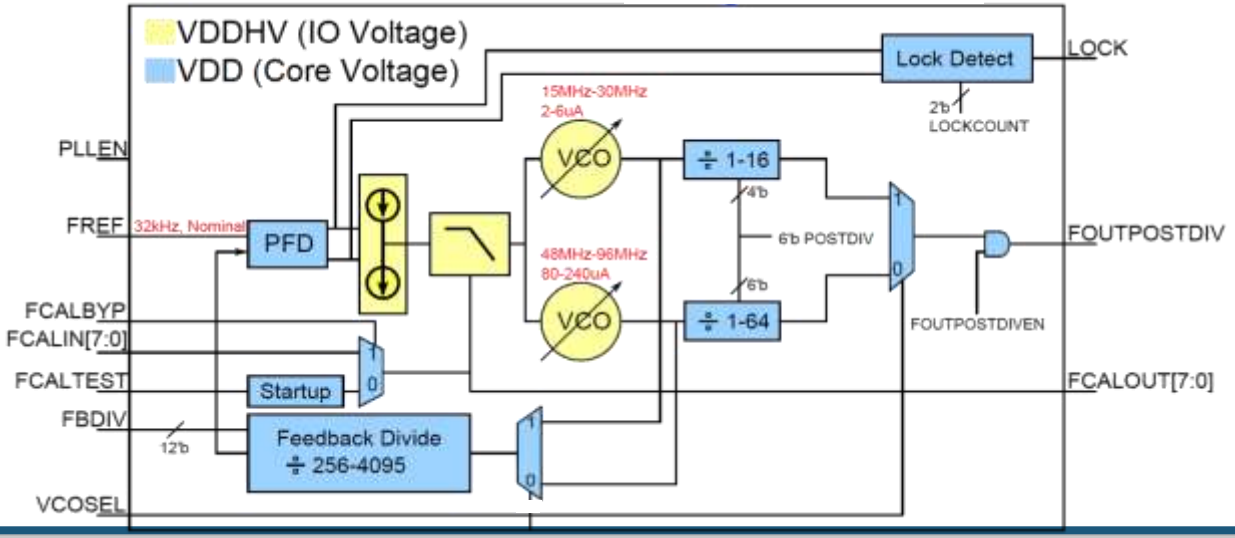
Clocking for “IoT”

- IoT = overused term, but useful shorthand for ultra-low power SoCs with
  - Low operating power
  - Able to start/stop quickly for low system power
  - Low leakage
  - Few/no external components

- Our clocking solutions leverage TSMC’s low-power process offering:
  - 180LP, 40ULP, 22ULL, and FinFET from 16nm to 5nm
  - PLLs with total power as low as 5µW and starting in as little as 3 reference clock cycles
  - Free-running oscillators with <2% total variation

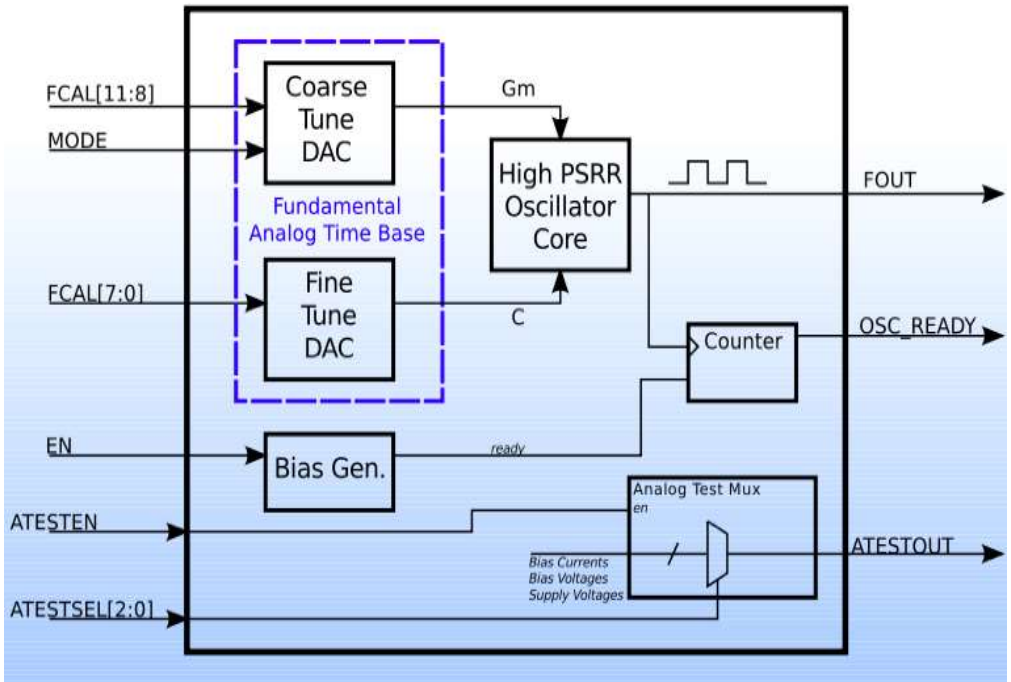
IoT PLL

- Extremely low power 32kHz RTC reference clock, as low as 5uW for whole PLL
- Starting – ±2% of freq. Cold in <1.2ms (40 cycles); Warm < 100us (3 cycles)
- 0.12mm2 and no external components
- Can include two VCOs – ultra-low power and decent jitter
- Production 10nm, 16nm, 40nm, 110nm; Proven 7nm, 28nm, 180nm



Free-running Oscillators

- Applications – watchdog timer, logic clock for ultra-low power mode (“IoT”)
- No external components
- 10nm, 28nm, 40nm, 65nm
- Possible (-40°C to 125°C, Vdd ±10%)
  - ±1.5% after trimming
  - Power < 30uW



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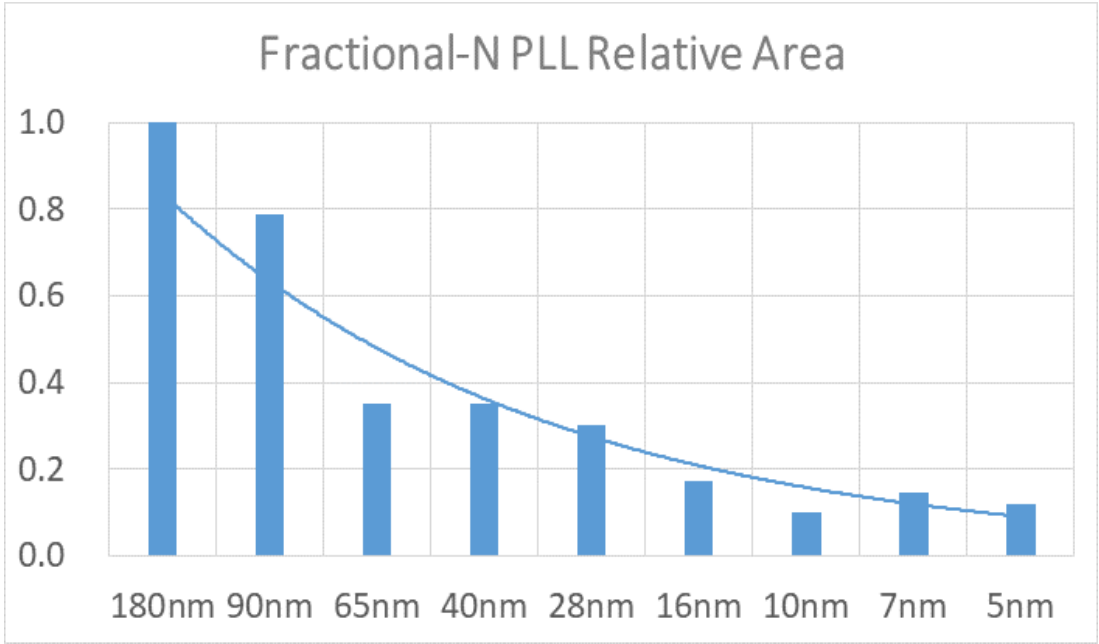
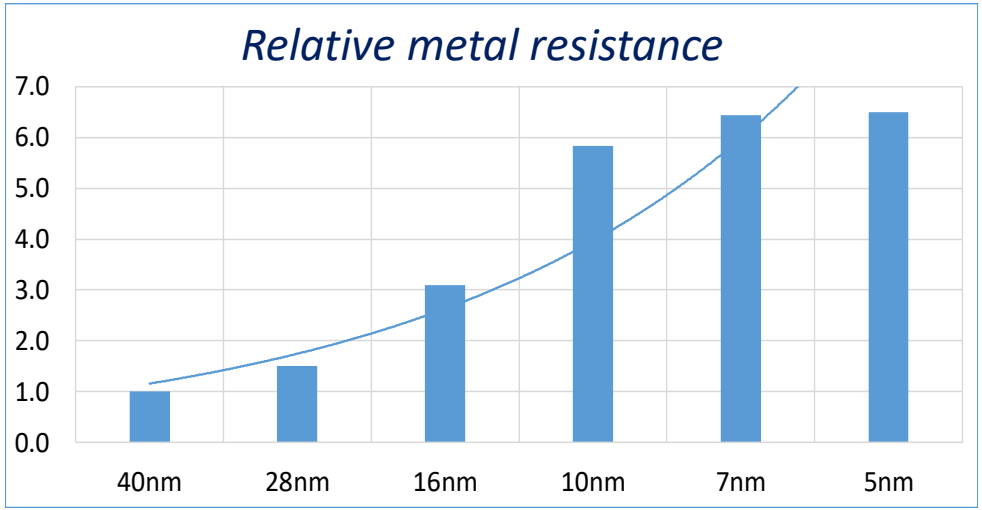
Analog scaling to 5nm

- Analog noise relates to kT/C, so area should scale with capacitance area
- It does! Analog scales, but less than digital
- From 180nm to 5nm:
  - Digital scaling ~800:1
  - Analog scaling ~8:1



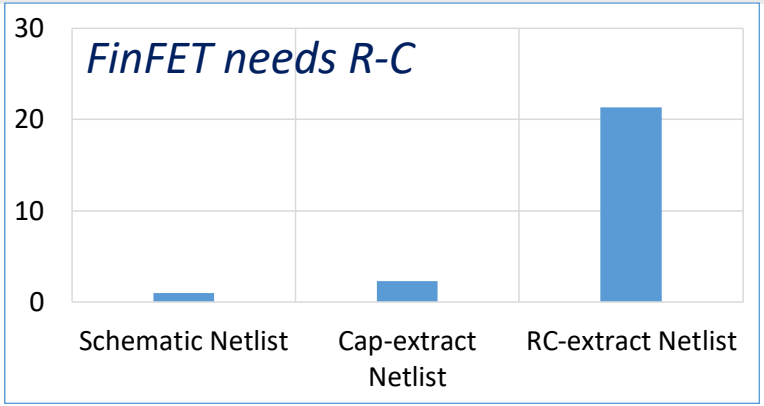
Wire resistance challenge

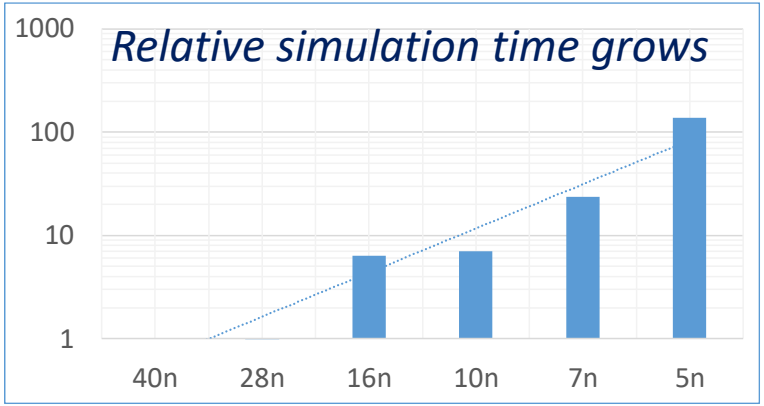
- Interconnect resistance is climbing quickly!
- Extraction and post extract simulations are becoming more important
- From 40nm to 5nm/7nm, wire resistance (Ω/sq) has risen ~6.5x
- Designs are increasingly difficult to verify due to the need for simulation of distributed RC parasitics



5nm Simulation Time

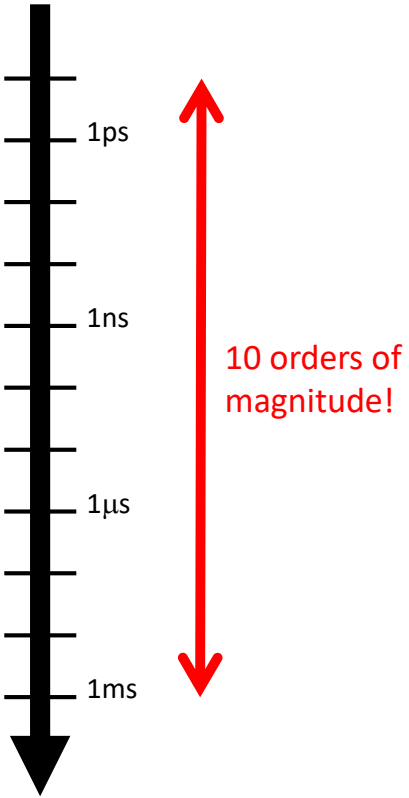
- Schematic sims are out, distributed
  C-C and R-C extracted simulations are essential
- Models are becoming more complex
  → Higher development costs:
  - Longer development cycles
  - Need parallel simulation and more CPU's
  - Need more EDA licenses





Timescale makes it worse

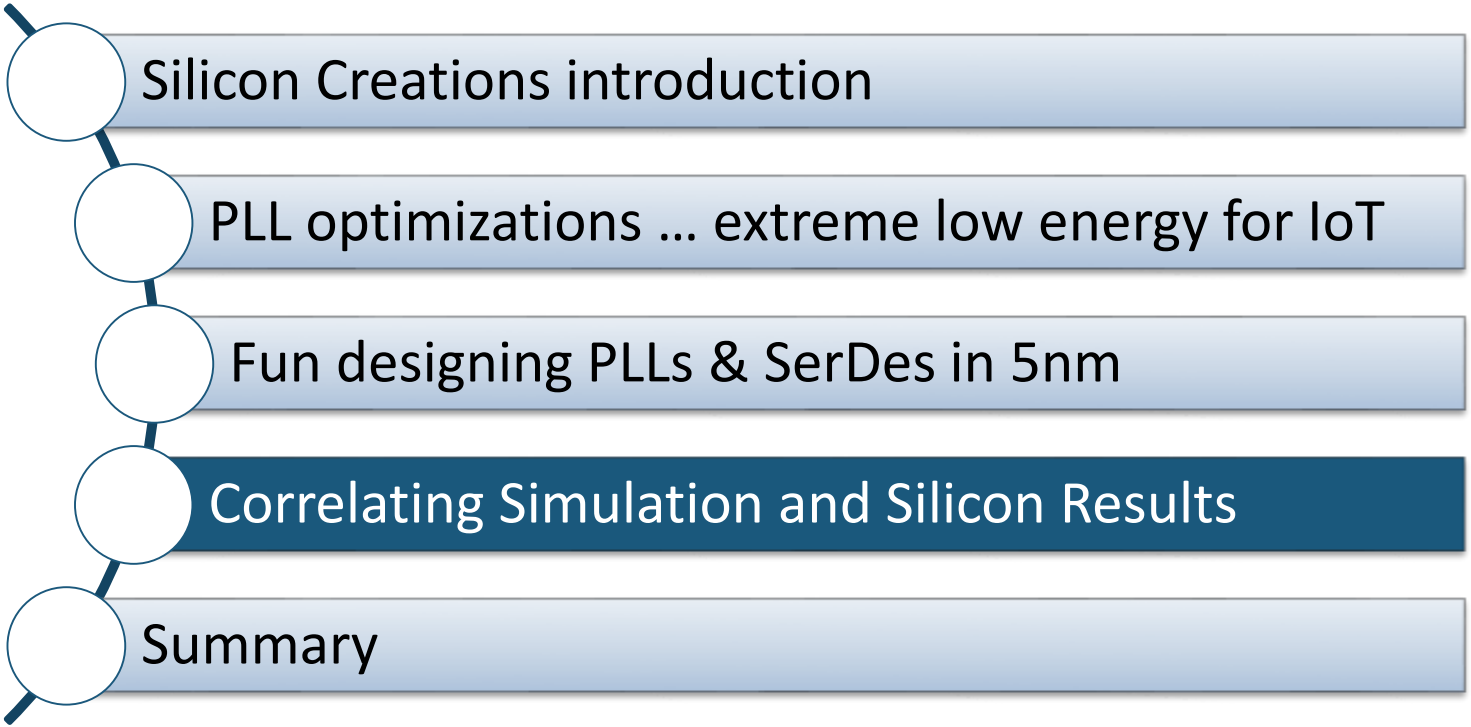
- Jitter requirements ~ 0.1ps
- Bit rates / clock cycle time ~100ps
- AC coupling time constant ~1us
- PLL lock time ~50us
- Link behavior ~1ms



5nm Computing Solution

- Distributed computing farm
  - >2200 CPU cores
  - >15TB RAM
- 1200 Simulation licenses
  - 200+ 16-core extracted sims
  - 300+ 4-core extracted sims
- Dedicated Calibre machines
  - Intel i9-7980XE 18-core 4.8GHz
  - CPU de-capped, water-cooled
  - 4 x 16GB DDR4 RAM
- Carrier 15 Ton Cooling Units
  - >50kW Capacity
- 140kW at full capacity!

Outline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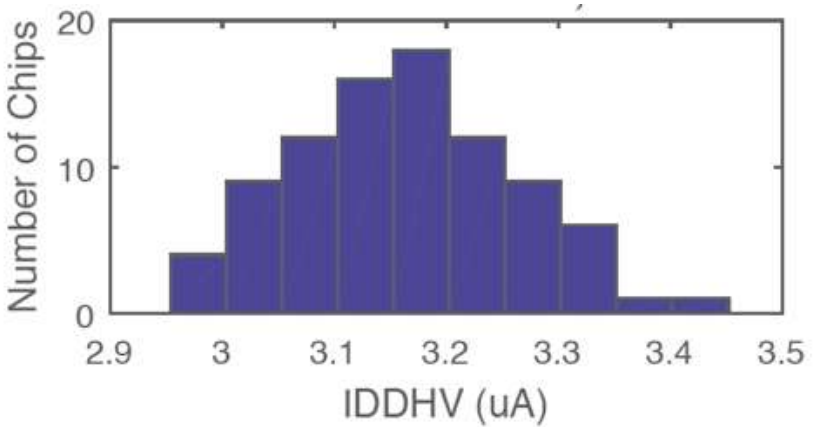
IoT PLL Power

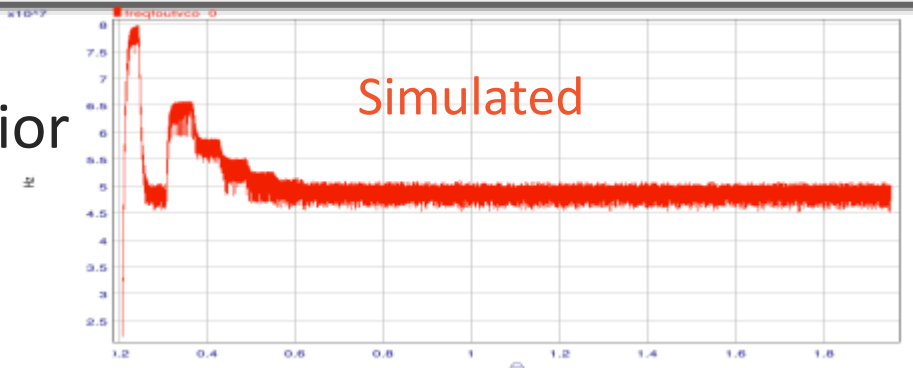
- **Simulation**
  - Mean=3.02uA
  - Stddev=1.5%
- **Measurement**
  - Mean=3.15uA
  - Stddev=1.6%

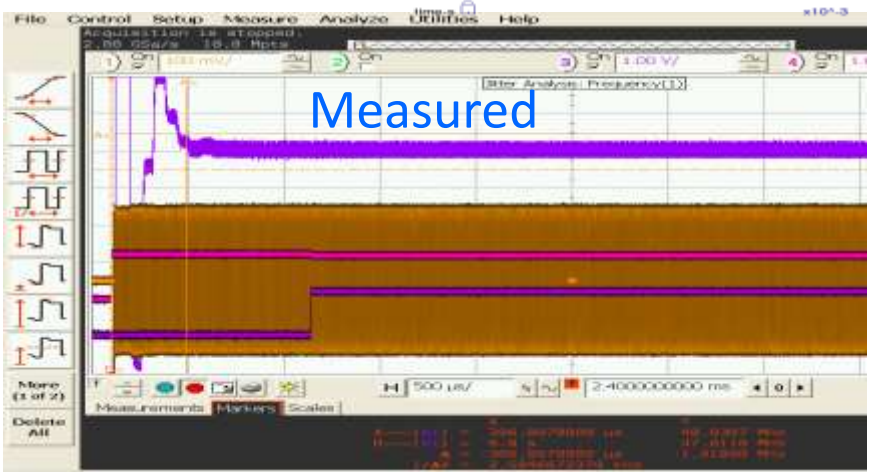
Measured Supply Current



IoT PLL Fast Locking

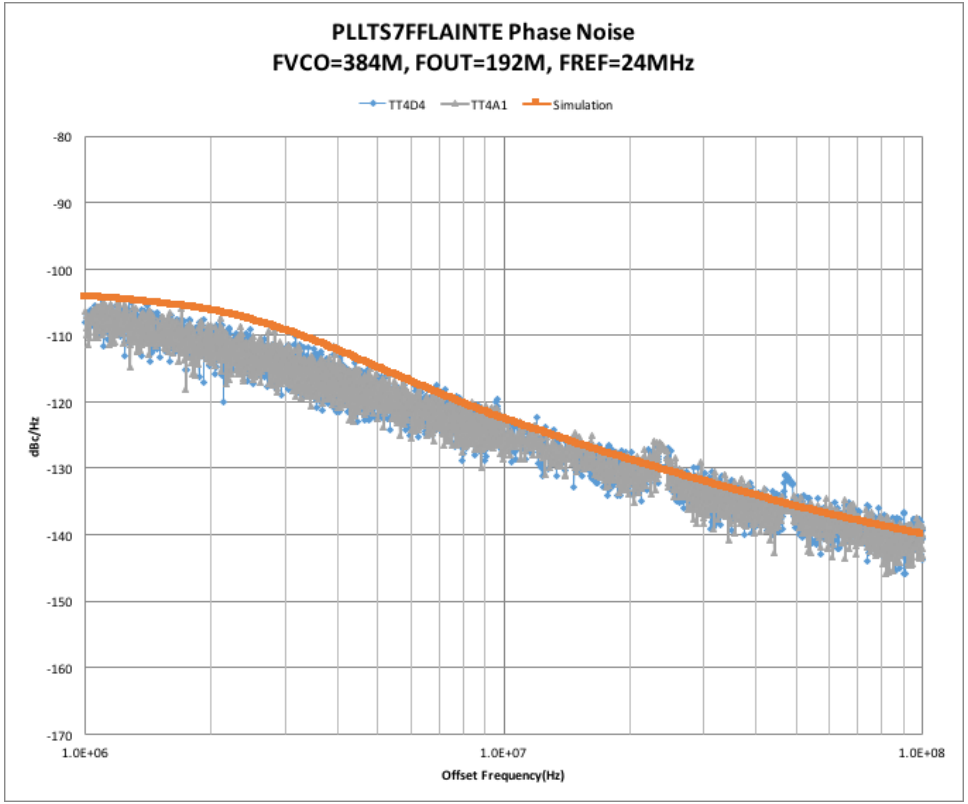
- AFS transient simulations accurately predict locking behavior (VCO frequency vs. time)
- 32kHz locking simulations must run for >1ms, so we need not only a fast locking PLL, but also
  - A fast simulator
  - Good SPICE models
  - Accurate extracted netlist (carefully reduced)





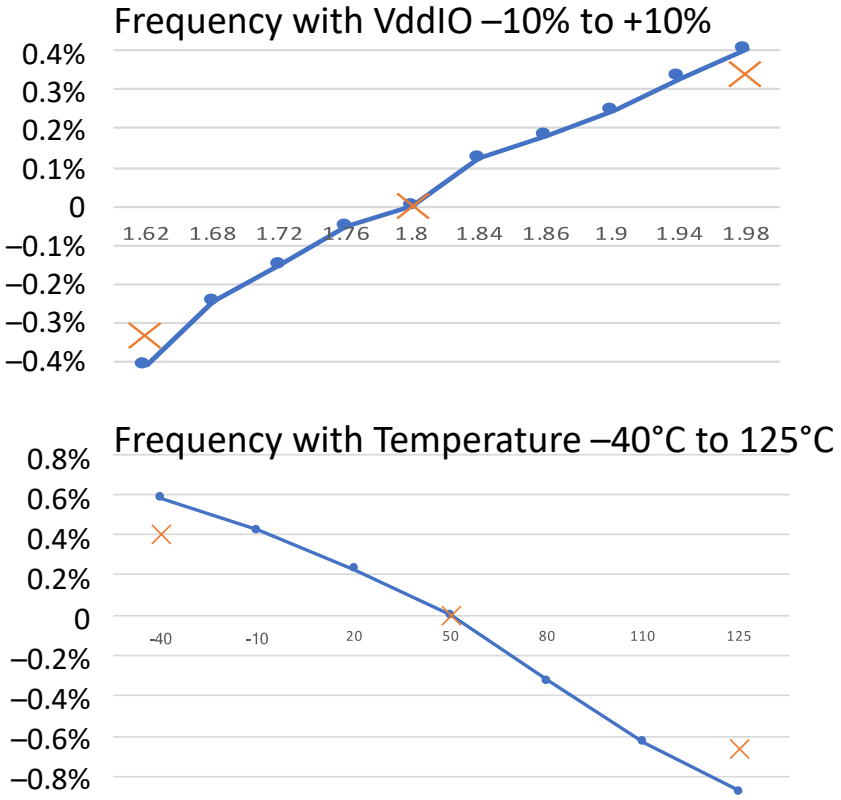
Phase Noise Correlation

- Ultra-Low Power (<100µW), Fast Locking PLL
- Phase noise (jitter) correlation achieved for PLLs with power from ~3µA to ~3mA



Oscillator Stability

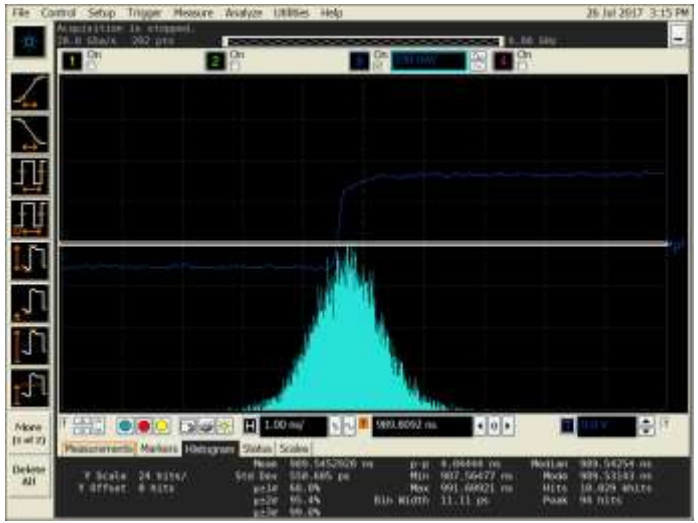
- Accurate frequency (without a crystal reference) across Voltage and Temperature variations



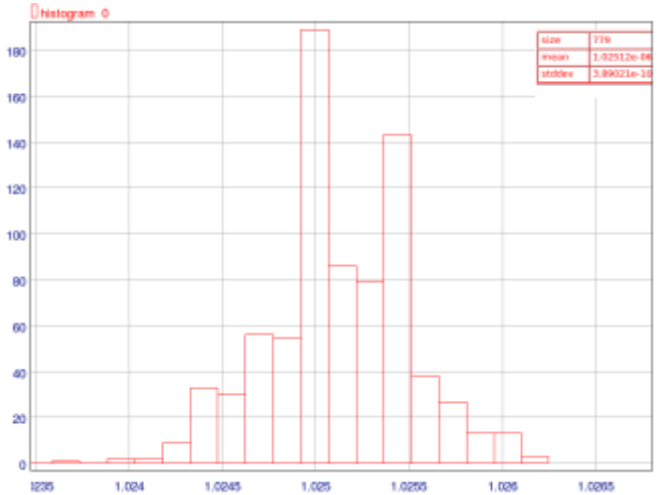
Oscillator Noise Correlation

- Highly non-linear, ultra-low power (<100µW), free-running oscillator is accurately modeled with AFS Transient Noise analysis

Measured OSCTS7FFRLXB – 0.55ns RMS



Simulated OSCTS7FFRLXB AFS
Trannoise Analysis: 0.39ns RMS



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Summary

- Silicon Creations has been providing reliable, high performance clocking and SerDes solutions to TSMC customers since 2006
- Designing for advanced FinFET is fun, but challenging and expensive
- With care, excellent correlations between simulations and first silicon have been shown in 7nm allowing production to start quickly
- Clocking solutions optimized for IoT contribute only a few uW to system energy and can be turned on and off quickly, yet can be designed for the target jitter
- 5nm solutions are taping out shortly