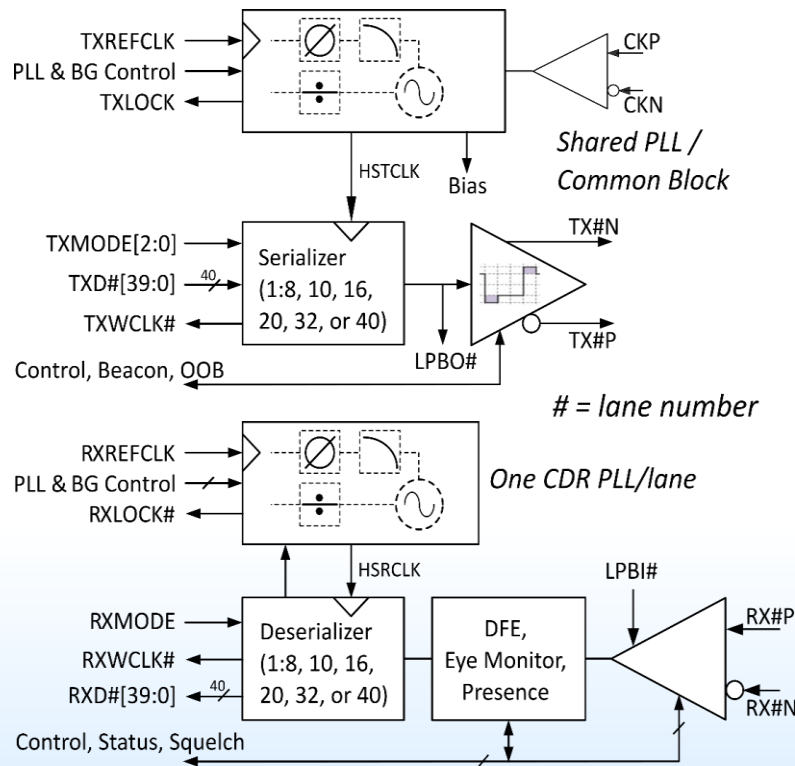


## Overview

Silicon Creations has a range of Serializer-Deserializer IP built upon proven ring PLLs and high-speed line drivers and receivers. Our PMA architecture is in production in over 25 SerDes, from 180nm to 6nm and at speeds up to 32.75Gbps. Our Multiprotocol PMA utilizes our proven PLL core making it very low power, widely programmable and compact.



## Features

- Supports over 30 protocols including PCIe, Ethernet 10G-X/S/K/R, DisplayPort, JESD204A/B/C, XAUI, SGMII, CEI 6G/11G SR/MR/LR, V-by-One, PON, OTN/OTU, 3GSDI, SAS1-3, SATA1-3
- 10/25GbE variant with 13UI in-PMA latency
- Robust ring-PLL based architecture
  - Low area – less than 1.2mm<sup>2</sup> for 4 Tx + 4 Rx
  - Low power – to 3pJ/bit
  - Extremely wide range: e.g. >100:1 from 125Mbps to 32.75Gbps in GF 12LP+
  - Extremely low jitter – measured <0.25ps RMS
- Tx PLL includes fractional multiplication, spread spectrum and Jitter Cleaner function for Sync-E and OTU
- Core-voltage line driver with programmable pre- and post-emphasis
- Out-of-band, electrical idle signaling capability for SAS, SATA, and PCIe
- Programmable CTLE and adaptive 5/14 - Tap Decision Feedback Equalizer for poor channels
- Eye monitor to measure eye opening at data slicer on chip

# Multiprotocol PMA

## Availability

Production TSMC 12/16FFC, 40LP/G, UMC 28HLP; GF 40LP;  
Silicon Proven GF 12LP+; TSMC 6FF; Taped out TSMC28HPC+ (to PCIe4)

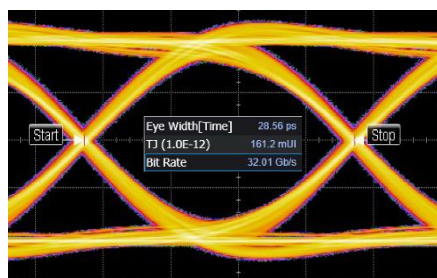
## Deliverables

- GDSII
- CDL Netlist
- Rich Verilog Model with Jitter and loop dynamics
- Verilog testbench incorporating BIST
- Liberty timing models (.lib)
- IBIS AMI models
- LEF layout abstract
- RTL wrapper for interface to controller including adaptive DFE; Optional PIPE PCS
- Comprehensive Application Note
- Industry leading support by IP designers
- Support for package design, Signal Integrity modeling and production test development

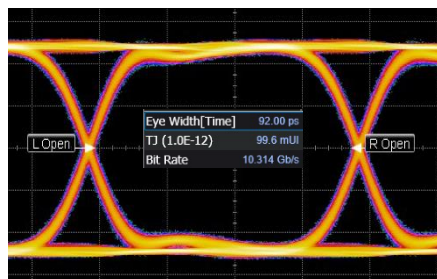
## Predictable and excellent performance

GF12LP+

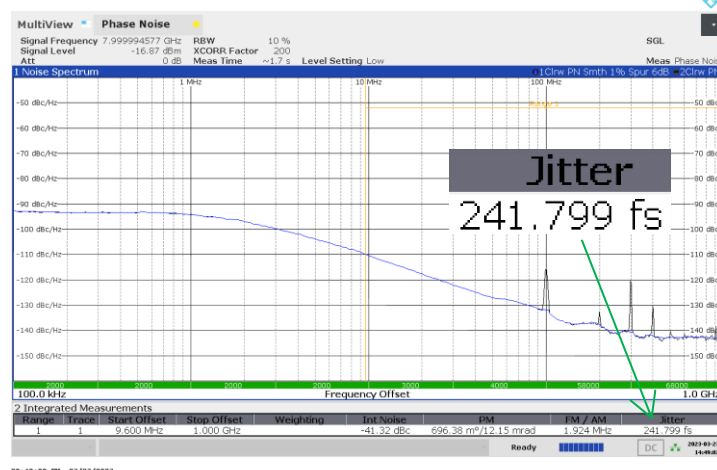
32Gbps  
Tx Eye  
1.6% UI TJ



10Gbps  
Tx Eye  
1% UI TJ



TSMC 12FFC PCIe4 Tx Output Phase Noise  
(D10.2 @ 16Gbps)



## About Silicon Creations

Silicon Creations is focused on providing world class silicon IP for precision and general purpose timing (PLLs), Chip-chip SerDes and high-speed differential IOs.

Our IP is in production from 3n to 180n. Our complete commitment to our customer success and our support will delight you. Our IP has an excellent record of first silicon to mass production in customers' designs. Our key designs have been comprehensively verified in our labs as well as in mass production with multiple customers.

Silicon Creations was founded in 2006, is self-funded and growing and is ISO9001. We have development centers in Atlanta, USA and Krakow, Poland and world-wide sales representation.

## Contact us

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- Email: [sales@siliconcr.com](mailto:sales@siliconcr.com)



## Related Information

[www.siliconcr.com](http://www.siliconcr.com)

- Products
- SerDes Interfaces

