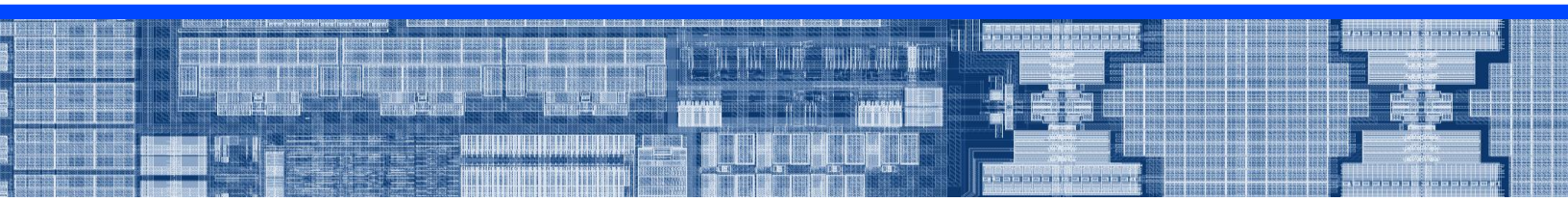
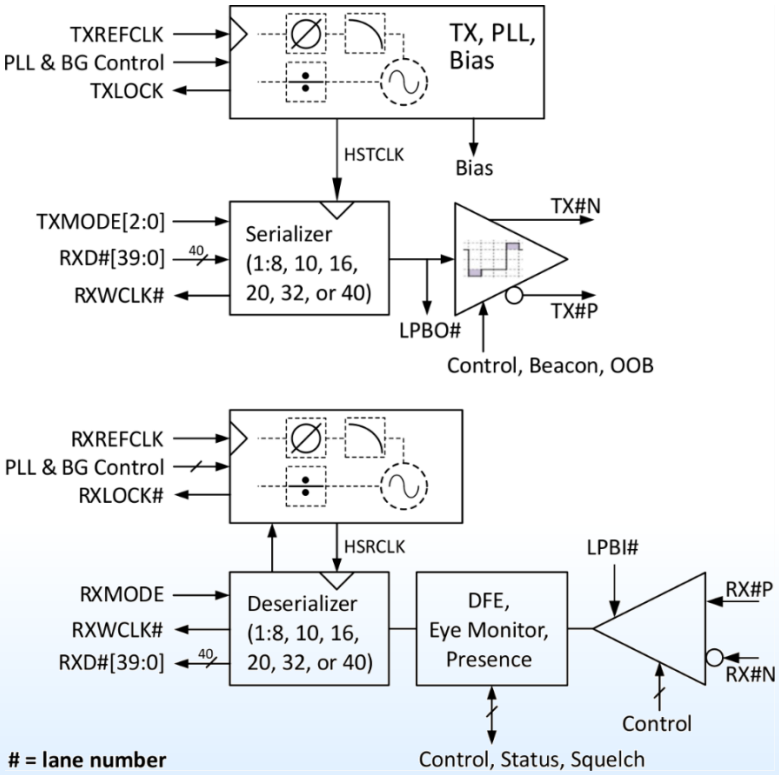
Silicon Creations

Multiprotocol PMA



Overview

Silicon Creations has a range of Serializer-Deserializer IP built upon proven ring PLLs and high-speed line drivers and receivers. Our PMA architecture is in production in over 25 SerDes, from 180n to 12n and at speeds up to 25Gbps. Our Multiprotocol PMA utilizes our proven PLL ring core making it very low power, widely programmable and compact.



Features

- Supports over 30 protocols including CEI 6G & 11G SR, MR, LR, Ethernet 10GBASE-X/S/K/R, PCIe Gen1/2/3/4, V-by-One HS, CPRI rates 1-9, PON, OTN/OTU, 3GSDI, JESD204A & B, SATA1-3, XAUI, SGMII
- Serialization width: 8, 10, 16, 20, 32, or 40 bit
- Robust ring-PLL based architecture
  - Low area – less than 1.3mm^2 for 4 Tx + 4 Rx
  - Low power – to below 4mW/Gbps/lane
  - Extremely wide range: E.g. >100:1 from 250Mbps to 16Gbps in TSMC 16 FFC
  - Extremely low jitter – measured <0.3ps RMS
- Tx PLL includes fractional multiplication, spread spectrum and Jitter Cleaner function for Sync-E and OTU
- Core-voltage line driver with programmable pre- and post-emphasis
- Termination programmable from 75Ω to 175Ω
- Out-of-band, electrical idle signaling capability for SAS, SATA, and PCIe
- Programmable CTLE and adaptive 5-Tap Decision Feedback Equalizer for poor channels
- Eye monitor to measure eye opening at data slicer on chip

Multiprotocol PMA

Availability

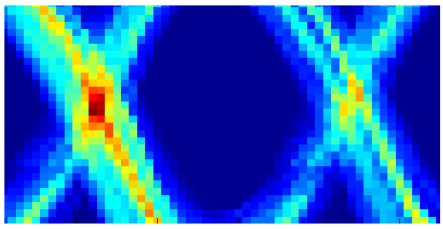
Production UMC 28 HLP; Silicon Proven TSMC 12FFC, 16FFC, 40 LP, 40 G and GLOBALFOUNDRIES 40 LP; 32.75Gbps GLOBALFOUNDRIES 12LP+ in development

Deliverables

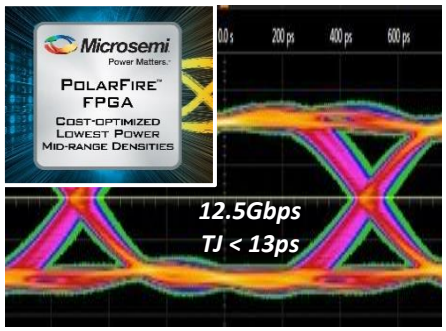
- GDSII
- CDL Netlist
- Rich Verilog Model with Jitter and loop dynamics
- Verilog testbench incorporating BIST
- Liberty timing models (.lib)
- IBIS AMI models
- LEF layout abstract
- RTL wrapper for interface to controller including adaptive DFE; Optional PIPE PCS
- Comprehensive Application Note
- Industry leading support by IP designers
- Support for package design, Signal Integrity modeling and production test development

Predictable and excellent performance

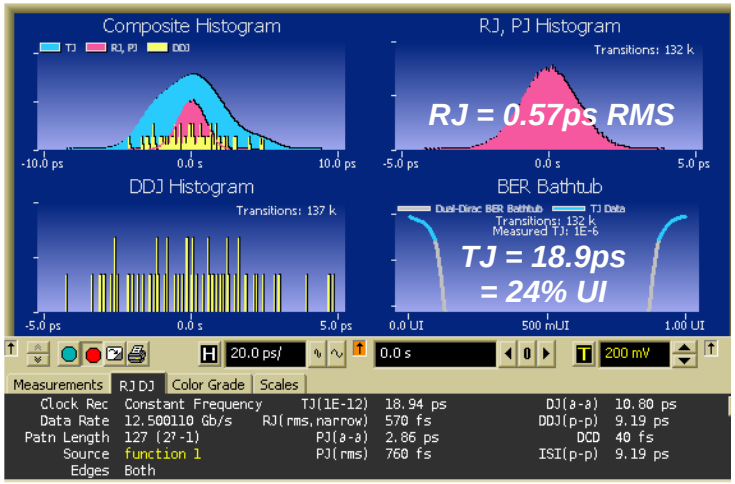
Rx Eye monitor DFE cleaned at 10.3125Gbps



Tx Eye diagram at 12.5Gbps (Microchip MP FPGA)



Tx Jitter decomposition at 12.5Gbps with 100MHz reference.



About Silicon Creations

Silicon Creations is focused on providing world class silicon IP for precision and general purpose timing (PLLs), Chip-chip SerDes and high-speed differential IOs.

Our IP is in production from 5n to 180n. Our complete commitment to our customer success and our support will delight you. Our IP has an excellent record of first silicon to mass production in customers' designs. Our key designs have been comprehensively verified in our labs as well as in mass production with multiple customers.

Silicon Creations was founded in 2006, is self-funded and growing. We have development centers in Atlanta, USA and Krakow, Poland and world-wide sales representation.

Contact us

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